Patent Claims

1. Data processing device with:

- a first circuit configuration (1), which connects a first communication bus (2) with a second communication bus (3) and is the bus master of the first communication bus (2);
- a second circuit configuration (4), which is connected with the first communication bus (2),

characterized by the fact that

the second circuit configuration is equipped with a first output port (5), which is connected with the input port (6) of the first circuit configuration (1).

2. Configuration in accordance with claim 1,

characterized by the fact that

a third circuit configuration (7) is arranged, which is equipped with a second output port (8) that is connected with the first output port (5) through a logical OR function (9), wherein the output port (10) of the OR function (9) is connected with the input port (6) of the first circuit configuration (1).

3. Configuration in accordance with one of the claims 1 or 2,

characterized by the fact that

the first circuit configuration (1) and the second circuit configuration (4) are separate integrated circuits, which are connected by the first communication bus (2) that is arranged on a system board.

4. Configuration in accordance with one of the claims 1 or 2,

characterized by the fact that

the first circuit configuration (1) and the second circuit configuration (4) are arranged in a joint integrated circuit.

5. Method for the operation of a data processing device with these steps:

- make a first circuit configuration (1) available that connects a first communication bus (2) with a second communication bus (3) and that is the bus master of the first communication bus (2), wherein a second circuit configuration (4) is connected with the first communication bus (2) and the second circuit configuration is equipped with an output port (5) that is connected with the input port (6) of the first circuit configuration (1),
- generate a wait signal (11) in the second circuit configuration (4);
- transmit the wait signal (11) from the second circuit configuration (4) to the first circuit configuration (1);
- allow the first circuit configuration (1) to wait until the second circuit configuration (4) ends the wait signal (11).

6. Method in accordance with claim 5,

characterized by the fact that

a third circuit configuration (7) is arranged, which is equipped with a second output port (8) that is connected with the first output port (5) through a logical OR function (9), wherein the wait signal (11) is sent from the output port (10) of the OR function (9) to the input port (6) of the first circuit configuration (1) as long as one of the circuit configurations (4, 7) transmits a wait signal.